INT-1010
TCP Offload Engine

Product brief, features and benefits summary

Highly customizable hardware IP block. Easily portable to ASIC flow, Xilinx or Altera FPGAs

INT-1010 is highly flexible that is customizable for layer-3, layer-4, layer-5 network infrastructure and network security systems applications. It is recommended for use in, among others, high performance Servers, NICs, SAN/NAS and data center applications. It provides the key IP building block for a single high performance Gigabit Ethernet ASIC/ASSP/FPGA.

INT-1010 provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others.

INT-1010 can process TCP/IP, for in-line network security appliances, sessions in both directions, simultaneously, at full G-bit rate. This relieves the host CPU from costly TCP/IP buffer stack execution and maintenance tasks.

INT-1010 can process TCP/IP sessions and has the capability to process other relevant protocols such as FTP, UDP, ICMP, TFTP etc on all inbound as well as outbound traffic simultaneously without compromising performance at sustained Gigabit speeds.

- Ideal for high performance and mid performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications

- Less than 4000 Xilinx slices, Altera ALMs or 150,000 ASIC gates + on-chip memory

- Fully integrated 100 Mbit/1-G bit high performance EMAC.

- Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.

- Hardware implementation of TCP/IP stacks’ control plane and data plane.

- Hardware implementation of ARP protocol.

ARP table creation, deletion management (optional)
• Customizable for IP-protocol only.

• On-chip DDR or SSRAM memory controller which can address from 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories (User customizable, optional)

• Many trade-offs for some functions performed in hardware or software

• Configurable Packet buffers, session table buffers On-chip or Off-chip memories, attached DDR I/II interface. Depending on system, performance, ASIC/FPGA size requirements—> User Customizable, (optional)

• Interfaces directly to GMII, RGMII, MII external 10/100/1000 Mbit Phy interfaces

• Architecture can be scaled up to 10-G bits

• Customizable to handle jumbo frames

• Generic bus interface for Local Processor control. ARM, PPC, MIPS and other CPU interfaces available

• User programmable/prioritize-able interrupts

• Performs connection/session management

• Monitors, Stores, Maintains and processes more than 4024 live TCP sessions. Customizable, depending upon on-chip memory availability.

• Extendable to 256K TCP sessions. Internal Memory dependent.

• Wire-speed 2Gbps performance at full duplex

• Can process up to 256K connections per second

• TCP + IP check sum generation and check performed in hardware in less than 6 clks (30 ns at 200 MHz) vs 1-2 us by typical software TCP-stack

• Connection set up and tear down/termination

• User programmable Session table parameters

• Dedicated set of hardware Timers for each TCP/IP session or customizable for sharing stale sessions.

• Multiple ‘slot storage’ for fragmented packets. More slots allocated when more On-chip Memory available. Self-checking available memory logic. (optional)

• Out of sequence packet detection/storage and Reassembly/Segmentation (optional)

• RDMA—Direct Data placement in Applications buffer at full
TCP Offload Engine- SoftCore IP

wire speed without CPU-> reduces CPU’s buffer copy time and utilization by 95%

- Future Proof- Flexible implementation of TCP Offload
- Accommodates future Specifications changes.
- Basic mini API available for PPC architecture. Others OSs/CPUs also available.

TCP/IP Offload/Accelerator Engine

Simplified Block Diagram
Specifications brief:

- Functionality Proven in multiple IDS/IPS appliances
- Complete header and flag processing of TCP/IP sessions in hardware → accelerates by 10 x – 50 x
- TCP Offload Engine- 2G b/s Wire-speed performance
- Scalable to 10 G b/s
- TCP + IP check sum- hardware
- TCP segmentation/reassembly in hardware
- Multiple ‘slot storage’ for fragmented packets
- Out of sequence packet detection/storage/Reassembly
- Accelerate security processing, Storage Networking-TCP
- RDMA- Data placement in Applications buffer
→ reduces CPU utilization by 90 %
- Future Proof- Flexible implementation of TCP Offload
- Accommodates future Specifications changes.
- TOE MS-chimney architecture compatible
- Customizable. Source code; Verilog

- Detailed specs available under NDA
## TCP Offload Engine - SoftCore IP

### Xilinx

![Xilinx board image]

### Altera

![Altera board image]

### ITOE Core Specifics - FPGA

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Altera Stratix III, IV, V, Virtex-II Pro(^1), Virtex-4, Virtex-5</th>
</tr>
</thead>
</table>
| Speed Grades  | • Stratix - 2 \(\approx 3256\)  
• -10 for Virtex-4 \(\approx 1256\)  
• -1 for Virtex-5 |
| Resources Used\(^2\) | Slices/ALMs | LUTs | FFs | Block RAM |
|                | ~2256 | ~3256 | ~1256 | 16-256 |

**Provided with Core**

| Documentation          | Product Specification  
User Guide  
Getting Started Guide |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Design File Formats</td>
<td>Alter-vqm, EDIF and NGC netlist</td>
</tr>
<tr>
<td>Constraints File</td>
<td>UCF</td>
</tr>
</tbody>
</table>
| Verification           | Verilog test bench  
Verilog test fixture |
| Example Design         | Verilog |

**Design Tool Requirements**

| Xilinx/Altera Implementation Tools | Quartus 8.1  
ISE\(^\text{\textregistered}\) v10.1 |
|-----------------------------------|----------------|
| Simulation                        | Mentor ModelSim\(^\text{\textregistered}\) v6.3c  
Cadence\(^\text{\textregistered}\) IUS v6.1  
Synopsys\(^\text{\textregistered}\) vcs_mxY-2006.06-SP1 |
| Synthesis                         | Quartus 8.1  
XST 10.1 |

---

*Intelop Corporation*  [www.intelop.com](http://www.intelop.com)
4800 Great America Pkwy. Ste-231
Santa Clara, CA. 95054  Ph: 408-496-0333, Fax: 408-496-0444