

25G Bit TCP Offload Engine (TOE) – INT 25011-*nnn* Hardware IP Core



*Enterprise Class, Network Hardened TCP/UDP Acceleration Technology,
Globally proven interoperability and rock solid reliability since 2009*

All Stages of Full TCP Stack in hardware plus more advanced functionality & features e.g. Fragmentation and out-of-sequence packet handling, Duplicate ACK/Fast Retransmit, TCP connection failure auto recovery and more.

25G bit-1K Sess TCP+UDP Offload + Host_IF

Series of TCP & UDP Accelerators in one single core with following product options:

25G, 1024 Sess = INT 25011-1K (Ultra-Low Latency USXTOE)

25G, 512 Sess = INT 25011-512 (Ultra-Low Latency USXTOE)

25G, 256 Sess = INT 25011-256 (Ultra-Low Latency USXTOE)

25G, 128 Sess = INT 25011-128 (Ultra-Low Latency USXTOE)

IP Cores for FPGAs and SoCs

Top Level Product Specifications

GOLD STANDARD IN TCP & UDP ACCELERATION

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Product brief, features and benefits summary:

Highly customizable hardware IP block. Easily portable to ASIC flow, Xilinx/Altera FPGAs or Structured/ASIC flow.

Eighth Generation TOE and System Solutions provide ‘Ultra-Low Latency’ and Ultra-High Performance with highest TCP bandwidth in Full Duplex. Network Tested and mature TCP protocol offload implementation

-All stages of Full TCP stack implemented in High performance hardware

- Ultra-Low Latency through 25 G TOE around 130+ ns
- Native 25G Architecture running at full 25G Network line rate
- Ultra-High Throughput: Receives and Sends sustained large TCP payloads, depending upon remote server/client’s capability.
- Fully Integrated and tested on Altera/Xilinx FPGAs; TOE+Host_I/F SoC IP bundle

INT 25011 is the only SOC IP Core that implements a full 25G bit TCP Stack in Handcrafted, Ultra-Low latency and High Performance, Innovative, Flexible and Scalable architecture which can also be easily customized for end product differentiation. It provides the lowest latency and highest performance in the industry. No exceptions.....

INT 25011 is the only SOC that integrates 25G TOE + Host interfaces in the smallest logic footprint. It is highly flexible that is customizable for layer-3, layer 4-7 network infrastructure and network security systems applications. It is recommended for use in, among others, high performance Cloud Servers, security appliances, Web Servers, Application servers, NICs, SAN/NAS and data center equipment design applications. It provides key IP building blocks for very high performance 25-Giga bit Ethernet ASIC/ASSP/FPGAs.

INT 25011 has built in advanced architectural flexibility that provides capability for enterprises to differentiate their Network security and Network infrastructure appliances from others and customize them for their specific design application.

INT 25011 can process TCP/IP sessions as client/server in mixed session mode for Network equipment and in-line network security appliances, simultaneously, at 25-G-bit rate. This relieves the host CPU from costly TCP/IP software related session setup/tear down, data copying and maintenance tasks thereby delivering 10x to 20x TCP/IP network performance improvement when compared with TCP/IP software.

INT 25011 also implements IGMP V1/V1/V3 protocol processing in hardware across all sessions. Available as an option to save BRAM and logic resources.

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Intilop offers a wide range of Full TOE processing hardware cores for 25/40GE to 1-GE applications. Use of PCI Express or embedded system interface is optional. TOE products support full TCP offload as well as conventional NIC mode operation (as an option in TCP Bypass Mode. The 25 G Bit TOE is based upon the proven and mature patent pending architecture from Intilop corporation.

TOE's design versions-

• Generic TOE for Network infrastructure design applications:

- a) 1014 Session with Payload FIFO of 8/16/32 K bytes
- b) 512 Session with Payload FIFO of 8/16/32 K bytes
- c) 256 Session with scalable Payload FIFO of 8/16/32 K bytes.
- d) 128 Session with scalable Payload FIFO of 8/16/32 K bytes
- e) Optional Very high performance DMA blocks also available to integrate with high performance PCIe Gen 2/3 interface.
- f) PCIe/Driver for Linux available as option

• TOE with enhanced Security features (available upon request)

- a) All of the options available in Generic TOE plus;
 - i. Protocol filter block can selectively direct traffic for any known application level protocol to any selected MAC port; e.g. all IM/chat traffic, SMTP (email), Web(http) traffic, VoIP etc. can be filtered and directed to selected ports.
 - ii. IP and Port number filter block
 - iii. Specific IP and Port Filtered traffic routed to optional selected MAC interface/s or PCIe interface or Memory interface directly at line rate without CPU involvement.
 - iv. MAC Filter block, traffic routed to any of the selected interfaces

Benefits of Intilop TOE:

Featuring APIs at different levels the General TOE allows the application developer to easily migrate from software, to TOE hardware, to custom hardware, to achieve higher performance.

Advantages and benefits:

- ~ 74G bit full duplex Throughput
- Very low application to application latency

APIs

Network applications use the Socket API. Typically OS implements the Socket API with a TCP/IP software stack. However, the Intilop TOE implements a standard Hardware API that bypasses the Kernel, places the user_payload data directly in user_space allowing next higher level applications to fully take advantage of TOEs full hardware Offload benefits.

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Optionally, to achieve higher performance, Intilop has implemented an equivalent Socket API named TOE Socket API through PCIe driver which enables plug and play acceleration through a simple intercept of legacy standard calls.

- Hardware API: Enables dedicated processing in the FPGA for application specific acceleration
 - Ideal for Very high performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications
 - Fully verified using comprehensive verification methodology for ASIC ports and Network system tested core.
 - Smallest logic foot print; less than 30,000 Xilinx slices, Altera ALMs or 250,000 ASIC gates + on-chip memory
 - Fully integrated 25 G bit high performance Ethernet MAC (optional)
 - Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.
 - Hardware implementation of TCP/IP stacks' control plane and data plane.
 - Hardware implementation of ARP protocol processing.
 - Extended ARP table creation, deletion management (optional)
 - Adheres to RFCs; 793, 1500, 1700, 813, 791, 2001
 - Fast Retransmit or Duplicate ACKs
 - Bypass mode (Acts as a NIC)
 - Hardware implementation of ICMP or Ping processing (opt)
 - Packet fragments and Out of Sequence packet handling
 - 'Sliding Window'. Similar mechanism implemented in hardware allowing Flow Control
 - 'Slow start' transfer control in hardware (opt)
 - Customizable for IP-protocol only.
 - Non-TCP Bypass mode lets all Non TCP/IP related traffic go directly to host interface via User_FIFO for TCP/IP software to handle
 - Can be deployed behind a gateway which will respond to Gateway-IP request as opposed to ARP request
 - On-chip DDR or SSRAM memory controller which can address from 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories (optional)
 - Simple User Side interface for easy hardware integration or a little more complicated for more power full and controlled 'Streaming' data transfers.
 - Many trade-offs for some functions performed in hardware or software

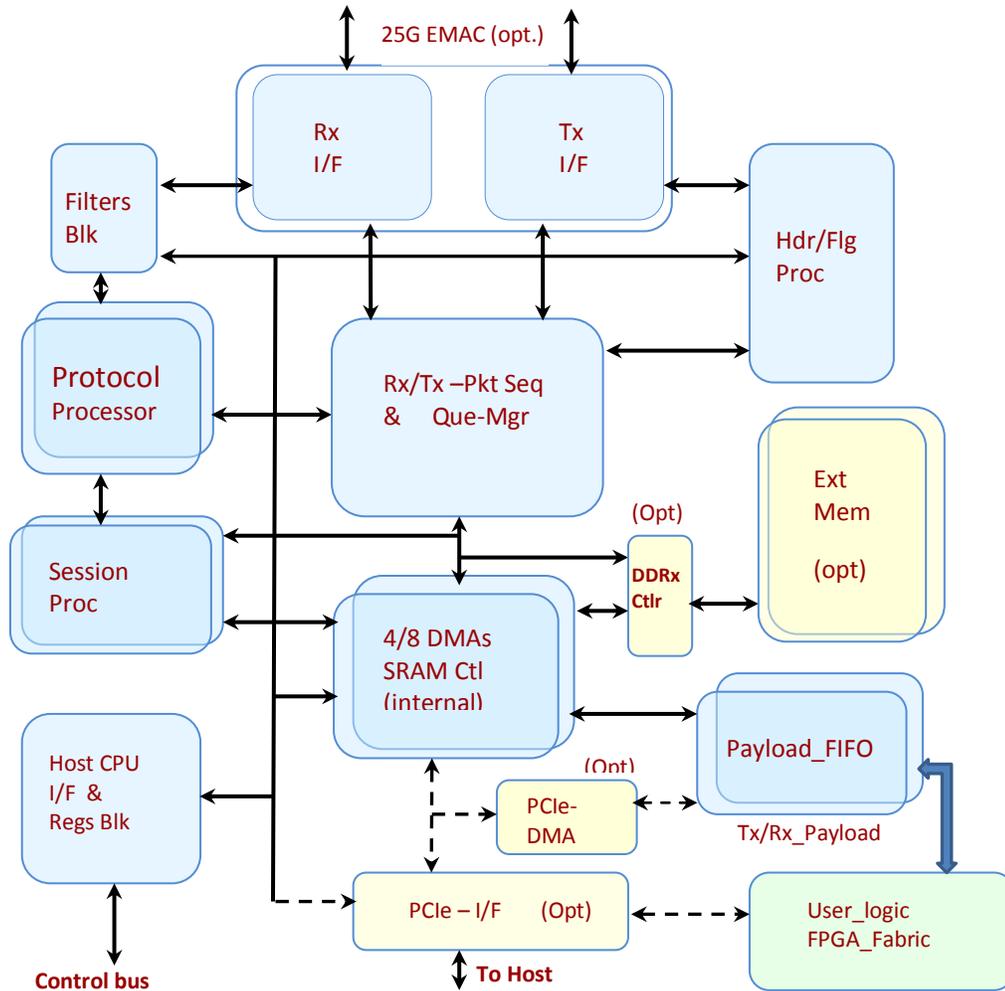
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- Configurable Packet buffers, session table buffers On-chip or Off-chip memories, attached DDR I/II interface. Depending on system, performance, ASIC/FPGA size requirements->
- Interfaces directly 25G MAC interfaces
- Customizable to handle jumbo frames
- Integrated PLB interface (Xilinx) or Altera Avalon. AXI bus interface available
- Integrated AMBA/Avalon 2.0 interface or MIPs CPU bus for Local Processor control
- User programmable/prioritize-able interrupts
- Performs connection/session management
- Monitors, Stores, Maintains and processes up to 1024 live TCP sessions. Customizable to implement more, depending upon on-chip memory availability and other FPGA limitations.
- Extendable to 16K TCP sessions. Internal Memory dependent.
- Wire-speed 74-Gbps Ethernet and TCP performance in full duplex
- Multiple TOEs can process up to 16K connections
- TCP + IP check sum generation and check performed in hardware in less than 6 clks (30 ns at 200 MHz) vs 1-2 us by typical software TCP-stack
- IGMP V1/V2/V3 support (opt)
- Connection Set up, tear down/termination and TCP data transfer without CPU involvement.
- User programmable Session table parameters
- Dedicated set of hardware Timers for each TCP/IP session (opt) or customizable for sharing one set of common timers for all stale sessions.
- Multiple 'slot storage' for fragmented packets. More slots allocated when more On-chip Memory available. Self-checking available memory logic. (optional)
- Out of sequence packet detection/storage and Reassembly/Segmentation (optional)
- Direct Data placement in Applications buffer at full wire speed without CPU-> reduces CPU's buffer copy time and utilization by 95%
- Support VLAN mode
- Easily customizable for filtering various IP and TCP traffic Protocols, directed towards any port or IP (Ideal for security appliances)
- Implements Full TCP/IP Offload. No CPU involvement at any TCP stage
- Future Proof- Flexible implementation of TCP Offload
- Fully integrated and FPGA ported PHY+MAC+TOE+PCIe/DMA System (opt)

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- Basic mini API available for easy integration with Linux/windows. Others OSs/CPU's also available
- Fully integrate System with PCIe/DMA and driver (optional)

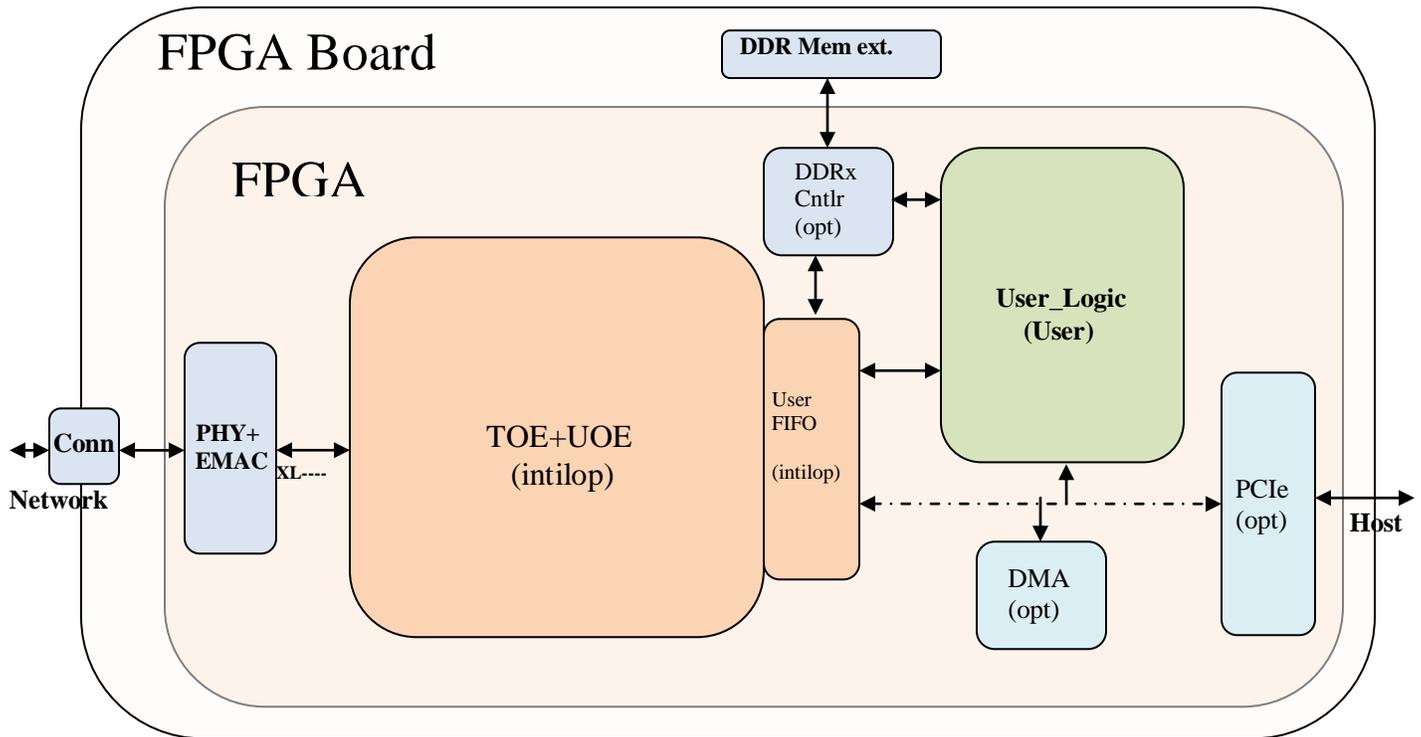
- EMAC+TOE+Host_Interface as one bundle SoC.
- Future TCP Specs updates easily adaptable



25G TCP Offload Engine (Simplified Block Diagram)

- Standard TOE
- TOE Options
- User Design

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FPGA Development System with fully integrated and tested; PHY+MAC+TOE+PCIe/DMA/Driver available as an option

Specifications brief:

- Fourth Gen-TOE. TCP Protocol Compliance and functionality proven in multiple networking equipment
- Complete header, flag processing of TCP/IP sessions and TCP Payloads in hardware → accelerates by 10x – 20x
- TCP Offload Engine- 25G b/s Wire-speed performance
- TCP + IP check sum- hardware
- All Retries implemented and managed by TOE without CPU involvement.
- TCP segmentation/reassembly in hardware
- Multiple ‘slot storage’ for fragmented packets (opt)
- Out of sequence packet detection/storage/Reassembly(opt)
- TCP port address tracking/automatic DMA
- MAC Address search logic/filter (opt)
- IP address search logic/filter (opt)
- Accelerate security processing, Storage Networking- TCP

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- **Direct Payload Data placement in Applications buffer in FPGA**
--> reduces CPU utilization by 95+ %
- **Future Proof- Flexible implementation of TCP Offload**
- **Accommodates future Specifications changes.**

AMBA/PLB/AXI CPU interface features;

- Basic transfers
- Various Transfer types
- Bus slave transactions
- Address decoder
- Bus Arbiter
- System Endianness: Little-Endian
- Master/slave Bus Arbitration (optional)

Deliverables:

- NetList. All TCP and or UDP configuration files, FPGA libs and many more
- Test Bench, ,vcd files, configuration code/API
- Verilog models for various components e.g. TCP/IP Client and Server models, transaction model (optional)
- External memory interface/model (optional).
- TCP Model (optional)
- Verification suite (optional)
- Test packet-traffic suite (optional)

CONTACT INTILOP FOR LATEST SPECIFICATIONS

(Specifications are subject to change)

Technology and Solutions License Purchasing Options:

- **IP Core in Netlist form.**
- **Fully ported and Network tested FPGA development Platforms**
- **IP Customization and Customer Hardware and Application Software integration services.**
- **Development Platforms available with boards from several board partners like Nallatech, Bittware, PLDA, HiTech Global, Terrasic and more.**

Contact intilop sales for details: info@intilop.com

