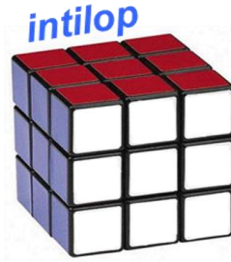


10 G Bit TCP Offload Engine (TOE-NIC) - X-Series- Fully Integrated FPGA board



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Very-High Performance System Solution

Fully integrated 10G bit
PHY+MAC+TOE+PCIe+DMA+Host_IF

On Select High End FPGA boards

SB 10G TOE-NIC (Very-Low Latency XTOE+PCIe-Board)

Top Level Product Specifications

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Most Reliable, Easiest and Fastest Time to Market cycle

System board with Fully Integrated Complex Mega-IP Cores, ported and network tested, running on Xilinx/Altera FPGAs. System provides ultra-high performance NIC functionality. Intilop employs best of the breed FPGA design, simulation and implementation tools and practices to accomplish this feat.

Board incorporates Third Generation TOE with ‘Very-Low Latency’ and Very-High Performance with very high TCP bandwidth in Full Duplex. Network Tested and mature TCP protocol offload implementation.

Board Key Features:

- Fully Integrated and Network tested System Solution running on Select Altera/Xilinx FPGA boards, providing; SXTOE+MAC+PHY+PCIe+DMA+Host_I/F SoC IP bundle.
- Fastest integration cycle and time to market; Just drop in your logic.
- Very-Low Latency through 10 G TOE = less than 200 ns
- Very-High Throughput: Receives and Sends sustained large TCP payloads, depending upon remote server/client’s capability.
- Benchmark Latency and Performance results for the full system available upon request.

Time to Market with minimal Risk:

SB 10G TOE-NIC is the only board that integrates a Full 10G TCP Offload Engine, Ethernet MAC, PHY-Layers, Host_CPU_I/F on Select Xilinx/Altera FPGA boards so customers can easily deploy their own differentiated design on an ultra-high performance FPGA board running their application. This allows them to save months of valuable engineering time and resources in porting complex set of IPs to a FPGA platform, instead they can simply concentrate on their own design for ultra-fast system implementation and time to market with minimum risk.

Intilop offers a wide range of Systems with Pre-integrated 10G and 1G TOE/UOE hardware cores for various end user applications. They include systems with Mutiple MAC+TOE, PCIe –Gen 2 or Gen 1 in x1/4/8 configurations, QDRx interfaces, DDRx interfaces and more. The standard System board features PCIe/DMA software driver and API that allows easy integration with customer’s applications running in Linux/host environment. This can also save them months of development time allowing them to concentrate on their own software application development.

SB 10G TOE-NIC is the only board that implements a full 10G bit PHY+MAC+TCP Full Offload Stack in Handcrafted, Ultra-Low latency and High Performance, flexible and scalable architecture which can also be easily customized for end product differentiation.

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***SB 10G TOE-NIC* is flexible and customizable for layer-3, layer 4-7 network infrastructure and network security systems applications. It is recommended for use in, among others, high performance Cloud Servers, Web Servers, Application servers, NICs, SAN/NAS, Network Security Appliances and data center equipment design applications. System contains Pre integrated and tested key IP building blocks for easy customer logic integration and deployment.**

Ultimate Performance Boost for your Network Bandwidth & ROI:

***SB 10G TOE-NIC* can process TCP/IP sessions as client/server in mixed session mode for Network equipment and in-line network security appliances, simultaneously, at 10-G-bit line rate. This relieves the host CPU from costly TCP/IP software related session setup/tear down, data copying and maintenance tasks thereby delivering 8x to 15x TCP/IP network performance improvement when compared with TCP/IP software.**

The 10 G Bit TOE is based upon the proven and mature patent pending TOE architecture from Intilop corporation.

The same architecture is scalable to 40 G bit.

System design versions-

- **Generic TOE for Network infrastructure design applications:**

- a) 16 Session with Payload FIFO of 8/16/32 K bytes
- b) 32 Session with Payload FIFO of 8/16/32 K bytes
- c) 64 Session with scalable Payload FIFO of 8/16/32 K bytes.
- d) 128 Session with scalable Payload FIFO of 8/16/32 K bytes
- e) 128+ Sessions depend upon on-chip BRAM
- f) Very high performance DMA blocks also available to integrate with high performance PCIe Gen 2 x 8 interface.
- g) PCIe/Driver for Linux

- **TOE with enhanced Security features (available upon request)**

- a) All of the options available in Generic TOE plus;
 - i. Protocol filter block can selectively direct traffic for any known application level protocol to any selected MAC port; e.g. all IM/chat traffic, SMTP (email), Web(http) traffic, VoIP etc. can be filtered and directed to selected ports.
 - ii. IP and Port number filter block
 - iii. Specific IP and Port Filtered traffic routed to optional selected MAC interface/s or PCIe interface or Memory interface directly at line rate without CPU involvement.

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- iv. MAC Filter block, traffic routed to any of the selected interfaces

Benefits of Intilop TOE:

Featuring APIs at different levels the General TOE allows the application developer to easily migrate from software, to TOE hardware, to custom hardware, to achieve higher performance.

Latency:

Board Latency Comparisons	Traditional NICs running TCP Software	Intilop H/W Acceleration
Wire to User_FIFO	10 – 20 us (in NICs with TOE)	400 – 500 ns (incl PHY+MAC+TOE)
Wire to Host Memory	30 – 40 us	1.5 – 6 us (Host+driver dependent)

- 20 G Ethernet Throughput.
- Scalable solution; 40G

APIs

Network applications use the Socket API. Typically OS implements the Socket API with a TCP/IP software stack. However, the Intilop TOE implements a standard Hardware API that bypasses the Kernel, places the user_payload data directly in user_space allowing next higher level applications to fully take advantage of TOEs full hardware Offload.

- Hardware API: Enables dedicated processing in the FPGA for application specific acceleration
 - Ideal for Very high performance specialized, differentiable ASICs or FPGAs for Network security or Network infrastructure applications
 - Fully verified using comprehensive verification methodology for ASIC ports and Network system tested core.
 - Smallest logic foot print; less than 30,000 Xilinx slices, Altera ALMs or 250,000 ASIC gates + on-chip memory
 - Fully integrated 10 G bit high performance Ethernet MAC. IEEE 802.3z compliant.
 - Scalable MAC Rx FIFOs and Tx FIFOs make it ideal for optimizing system performance.
 - Hardware implementation of TCP/IP stacks' control plane and data plane.
 - Hardware implementation of ARP protocol processing.
 - Extended ARP table creation, deletion management (optional)
 - Adheres to RFCs; 793, 1500, 1700, 813, 791, 2001

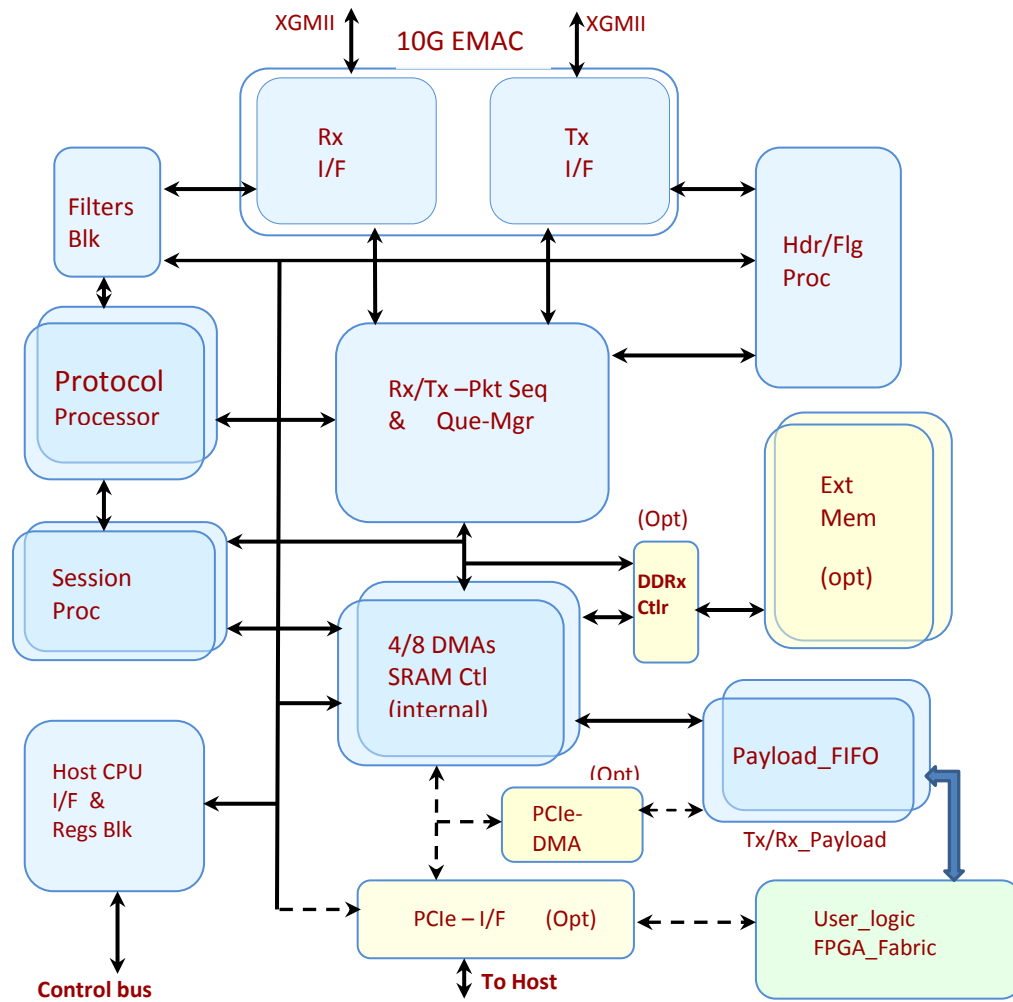
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- Hardware implementation of ICMP or Ping processing.
- ‘Sliding Window’. Similar mechanism implemented in hardware allowing Flow Control
- ‘Slow start’ transfer control in hardware (opt)
- Customizable for IP-protocol only.
- Non-TCP Bypass mode lets all Non TCP/IP related traffic go directly to host interface via User_FIFO for TCP/IP software to handle
 - Can be deployed behind a gateway which will respond to Gateway-IP request as opposed to ARP request
 - On-chip DDR or SSRAM memory controller which can address from 4K Bytes to 4 MB Bytes on chip or 256 MB off chip memories (optional)
 - Simple User Side interface for easy hardware integration or a little more complicated for more power full and controlled ‘Streaming’ data transfers.
- Many trade-offs for some functions performed in hardware or software
- Configurable Packet buffers, session table buffers On-chip or Off-chip memories, attached DDR I/II interface. Depending on system, performance, ASIC/FPGA size requirements-> **User Customizable, (optional)**
- Interfaces directly to XGMII, 10 G Bit serial interfaces
- Customizable to handle jumbo frames
- Integrated PLB interface (Xilinx) or Altera PLB. AXI bus interface available
- Integrated AMBA 2.0 interface or MIPS CPU bus for Local Processor control. (opt)
- User programmable/prioritize-able interrupts
- Performs connection/session management
- Monitors, Stores, Maintains and processes up to 1024 live TCP sessions. Customizable to implement more, depending upon on-chip memory availability and other FPGA limitations.
- Extendable to 4K TCP sessions. Internal Memory dependent.
- Wire-speed 20-Gbps Ethernet and TCP performance in full duplex
- Multiple TOEs can process up to 4K connections per second
- TCP + IP check sum generation and check performed in hardware in less than 6 clks (30 ns at 200 MHz) vs 1-2 us by typical software TCP-stack
- Connection Set up, tear down/termination and TCP data transfer without CPU involvement.
- User programmable Session table parameters

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- Dedicated set of hardware Timers for each TCP/IP session (opt) or customizable for sharing one set of common timers for all stale sessions.
- Multiple 'slot storage' for fragmented packets. More slots allocated when more On-chip Memory available. Self-checking available memory logic. (optional)
- Out of sequence packet detection/storage and Reassembly/Segmentation (optional)
- Direct Data placement in Applications buffer at full wire speed without CPU-> reduces CPU's buffer copy time and utilization by 95%
- Support VLAN mode (optional)
- Easily customizable for filtering various IP and TCP traffic Protocols, directed towards any port or IP (Ideal for security appliances)
- Implements Full TCP/IP Offload. No CPU involvement at any TCP stage
- Future Proof- Flexible implementation of TCP Offload
- Fully integrated and FPGA ported PHY+MAC+TOE+PCIe/DMA System (opt)
- Basic mini API available for easy integration with Linux/windows. Others OSs/CPU's also available
- Fully integrate System with PCIe/DMA and driver (optional)
- EMAC+TOE+Host_Interface as one bundle SoC.
- Standard Simple Streaming Data interface at Rx/Tx User_FIFOs
- Future TCP Specs updates easily adaptable

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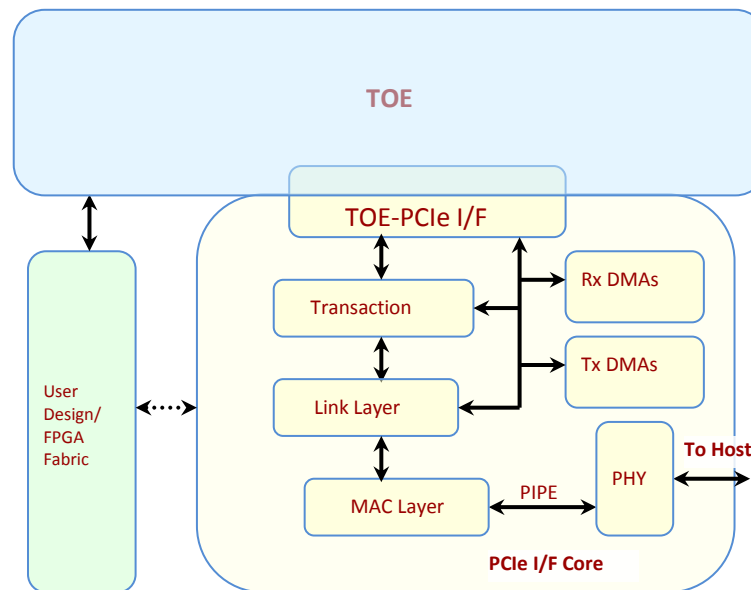
10G TCP Offload Engine + EMAC (Simplified Block Diagram)

- Standard TOE
- TOE Options
- User Design

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PCI Express IP core and TOE+PCIe FPGA NIC Key features:

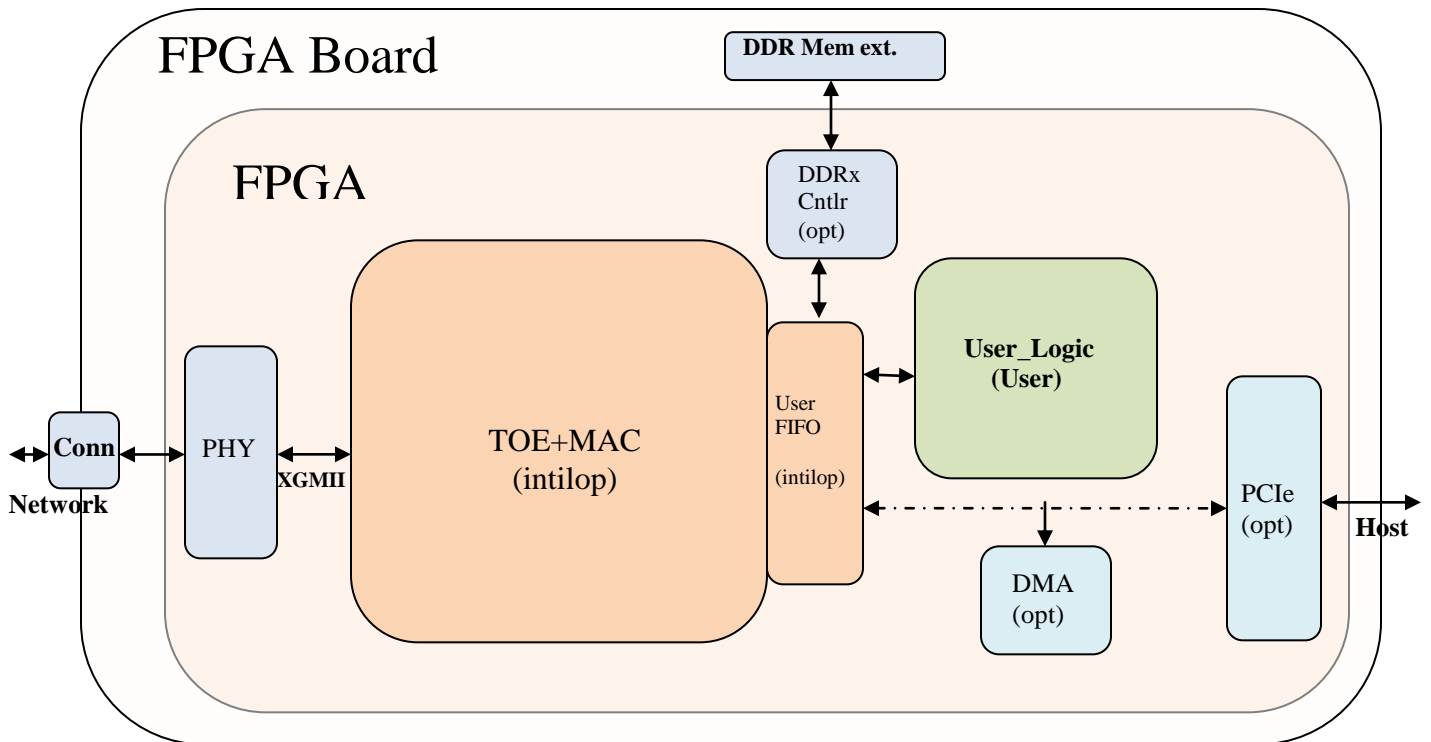
- Compliant with the PCI Express® Base Specification, revision 2.0 and 1.1
- Supports Native and Legacy Endpoint: x1, x4, x8 lanes
 - 1 Virtual Channel (VC) with standard TOE+DMA+PCIe NIC System
 - Up to 32 PCIe Virtual Channels available as Option
- Direct TOE Register access via PCIe interface.
- Dedicated and independent high performance TCP Payload Data Path between TOE and PCIe
- TOE-PCIe driver API for easy Linux Host System Application integration
- Standard TOE+PCIe+DMA FPGA-NIC implements up to 4 DMAs.
- Includes Physical, Data Link, Transaction, and EZDMA Application layers
 - Optimized for high throughput and minimal latency
- PIPE interface to PHY
 - 16-bit/125Mhz or 8-bit/250Mhz
- Maximum payload size up to 2KB
- Number of outstanding read requests: up to 16
- Up to 6 BARs plus expansion ROM
- DMA-based user's interface
 - Up to 8 DMA channel option
 - Scatter-Gather support with host based descriptors
 - Integrated DMA arbitration optimized for maximum throughput
 - PCIe Standard Linux Driver with fully Integrated FPGA-NIC-System/development Kit
- Ultra-High Performance, Ultra-low latency PCIe driver with fully Integrated FPGA-NIC-System/development Kit, available as Option



TOE + DMA + PCIe (Simplified Diagram)

□ Standard TOE □ TOE Options □ User Design

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**FPGA Board System with fully integrated and tested;
PHY+MAC+TOE+PCIe+DMA+Host_IF, available on select boards from intilop
board partners**

Contact: info@intilop for more details

Board and FPGA Specifications available at:

FPGA Vendors: www.Altera.com

www.Xilinx.com

Board Vendors: www.bittware.com

www.hitechglobal.com

www.Nallatech.com

www.plda.com

www.terasic.com

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Deliverables:

- FPGA board/Project files.
- IP NetList.
- System Networking test software.
- Test Bench, ,vcd files, configuration code/API for easy Linux port
- Verilog models for various components e.g. TCP/IP Client and Server models, transaction model (optional)
- External memory interface/model (optional).
- TCP Model (optional)
- Verification suite (optional)
- Test packet-traffic suite (optional)

CONTACT: info@intilop.com for latest system Specifications

Full FPGA Solutions License Purchasing Options:

- **Fully Integrated/Ported IP cores and Network tested FPGA development System Platform with specified interface options**
- **IP Customization and Customer Hardware and or Application Software integration services.**

Contact sales@intilop.com for details

